AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all previous versions, and listings, of claims in the application.

Listing Of Claims:

Claims 1-9. (Cancelled).

Claim 10. (Previously presented) A single-chip audio/video encoder device comprising, on a single integrated circuit:

multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio;

a first encoder that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;

wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and

wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

Claim 11. (Previously presented) The device according to claim 10, wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder.

Claim 12. (Previously presented) The device according to claim 10, wherein the first encoder and the second encoder operate concurrently.

Claim 13. (Previously presented) The device according to claim 10, wherein the first encoder and the second encoder perform luminance and chrominance filtering.

Claim 14. (Previously presented) The device according to claim 10, wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data.

Claim 15. (Previously presented) The device according to claim 10, wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals.

Claim 16. (Previously presented) The device according to claim 15, wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface.

Claim 17. (Previously presented) The device according to claim 15, wherein the at least one bus interface is configurable to act as a bus master using direct memory access.

Claim 18. (Previously presented) The device according to claim 15, wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

Claim 19. (Previously presented) The device according to claim 15, wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface.

Claim 20. (Previously presented) The device according to claim 10, wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels.

Claim 21. (Previously presented) The device according to claim 10, wherein the first encoder and the second encoder each comprise a plurality of search processors for performing motion analysis.

Claim 22. (Previously presented) The device according to claim 21, wherein the plurality of search processors operate in parallel, each upon a different portion of a macroblock.

Claim 23. (Previously presented) The device according to claim 21, wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions.

Claim 24. (Previously presented) A single-chip audio/video encoder device comprising, on a single integrated circuit:

control circuitry that synchronizes a first encoder, a second encoder, and multiplexing circuitry to produce a first multiplexed stream from first uncompressed video data, first uncompressed audio data, second uncompressed video data, and second uncompressed audio data, when the multiplexing circuitry operates in a first mode, and to concurrently produce the first multiplexed stream from the first uncompressed video data and the first uncompressed audio data and a second multiplexed stream from the second uncompressed video data and the second uncompressed audio data, when the multiplexing circuitry operates in a second operating mode;

a first input for receiving the first uncompressed video data and first uncompressed audio data from a first source external to the device;

a second input for receiving second uncompressed video data and second uncompressed audio data from a second source external to the device;

wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and

wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

Claim 25. (Previously presented) The device according to claim 24, wherein the encoding of the first multiplexed stream and the encoding of the second multiplexed stream is performed concurrently.

Claim 26. (Previously presented) The device according to claim 24, wherein encoding of one or both of the first uncompressed video data and/or the second uncompressed video data comprises luminance and chrominance filtering.

Claim 27. (Previously presented) The device according to claim 24, wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data.

Claim 28. (Previously presented) The device according to claim 24, wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals.

Claim 29. (Previously presented) The device according to claim 28, wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface.

Claim 30. (Previously presented) The device according to claim 28, wherein the at least one bus interface is configurable to act as a bus master using direct memory access.

Claim 31. (Previously presented) The device according to claim 28, wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

Claim 32. (Previously presented) The device according to claim 28, wherein encoding and/or multiplexing is performed by microcode instructions received by the device via the at least one bus interface.

Claim 33. (Previously presented) The device according to claim 24, wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels.

Claim 34. (Previously presented) The device according to claim 24, wherein the encoding of one or both of the first uncompressed video data and/or the second uncompressed video data is performed by a plurality of search processors for performing motion analysis.

Claim 35. (Previously presented) The device according to claim 34, wherein the plurality of search processors operate in parallel, each upon a different portion of a macroblock.

Claim 36. (Previously presented) The device according to claim 34, wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions.